



Image processing with high-speed and low-energy approximate arithmetic circuit

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ABSTRACT

Nowadays there are plenty of compute-intensive algorithms that are carried out at the edge. Therefore, it is necessary to design low-energy and high-speed circuits. Approximate computing (AC) is an emerging paradigm that can be used in error-resilient applications such as multimedia processing. In this paper, a novel approximate full adder design is proposed with the aim of latency and energy consumption reduction at the cost of producing some errors at the output. The proposed design uses pass transistor and transmission gate logic styles to achieve these aims. The proposed cell and referenced circuits are applied in a vast range of simulation conditions including power supply, ambient temperature, and load variations. Moreover, the constancy of the proposed cell concerning the process variations of carbon nanotubes (CNTs) is studied. All circuits are implemented at the transistor level using carbon nanotube field-effect transistor (CNFET) technology. Experimental results based on HSPICE simulation indicate the superiority of the proposed cell in terms of latency, power-delay product (PDP), and energy-delay product (EDP) criteria against state-of-the-art designs. Moreover, at the application level, image blending is used to study the accuracy metrics such as peak signal-to-noise ratio (PSNR) and structural similarity (SSIM) quantitative metrics. Finally, the PDP, PSNR, and SSIM metrics are simultaneously taken into account as a figure of merit (FOM) to trade-off between circuit and application-level metrics. Quantitative results confirm the better functionality of the proposed approximate full adder cell compared to its counterparts.

1. Introduction

For the time being, we are observing the widespread growth of the edge computing applications and portable consumer electronics such as Internet of Things (IoT) devices, laptops, notebooks, cell phones, smartwatches, and personal digital assistants (PDAs) that demand low power consumption and high-performance circuits [1,2]. Many of these devices typically perform complex computational operations such as data mining, machine learning, pattern recognition, neuromorphic systems, and multimedia processing algorithms [3]. Sophisticated computational operations result in more power being consumed in very large-scale integration (VLSI) digital systems. Therefore, the battery dies soon and it should be recharged again. According to the report of the Cisco Global Cloud Index, IoT-based systems and human beings will produce approximately 850 ZB data by 2021, and there is a limited power budget to process this amount of data [4]. Therefore, it is

inevitable to design high-speed and low-power circuits to alleviate this problem to some extent. Digital signal processing (DSP) cores and arithmetic logic units (ALUs) are the backbone of portable digital systems. The well-known 1-bit full adder cell is extensively used within computational units as their building blocks. It is also used to design larger and more complex arithmetic circuits such as subtractor, multiplier, and divider. These complex circuits, in turn, are used to realize digital signal processing algorithms such as different kinds of filters, multimedia or machine learning algorithms. Therefore, the design of low-power and high-speed full adder cells plays an important role in determining the performance of the entire digital system [5]. Many of the above-mentioned applications, including multimedia (image, audio, or video) processing, do not require accurate outputs and are resistant to computational errors [6]. Human limited perception cannot detect output errors readily. Therefore, the approximate computing (AC) method can be efficiently employed to design highly efficient circuits

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[7]. Improving power consumption and latency of a digital system can be carried out at various abstraction levels such as algorithm [8], architecture [9], gate [10], and transistor [11].

Moore's Law was introduced in 1965 and states that the number of transistors per unit area of the silicon chip almost doubles every two years [12]. According to Moore's Law, the dimensions of transistors have been continuously decreasing, leading to smaller transistors. In 2006, the gate length of the transistors was downsized to 65 nm, and semiconductor technology entered the nano era [13]. Metal oxide semiconductor field-effect transistors (MOSFETs) encounter serious problems in the nanoscale that disrupt their downsizing process further. For instance, drain-induced barrier lowering (DIBL), short channel effects, decreased gate controllability, hot electron effect, surface scattering, large process variation, soft errors, and off-leakage current are some of them [14–17]. Due to physical limitations, the shrinking of the transistors will eventually stop. Therefore, various technologies have been proposed to replace the traditional MOSFET technology such as quantum-dot cellular automata (QCA) [18], single-electron transistor (SET) [19], fin field-effect transistor (FinFET) [20], Spintronic [21], and carbon nanotube field-effect transistor (CNFET) [22].

The CNFET technology, due to its outstanding features, has attracted significant attention for designing high-performance and low-power digital circuits. It has been considered as one of the alternatives to replace traditional complementary metal-oxide-semiconductor (CMOS) technology. In the following, we describe some of the unique features of the CNFET devices. Similar to MOSFETs, CNFET devices comprise p- and n-type transistors called PCNFET and NCNFET, respectively. Unlike MOSFET transistors, PCNFET and NCNFET transistors with the same dimensions have the same mobility, which makes the sizing of complex circuits easier. Another benefit is that the current-voltage (I-V) characteristics of CNFETs and MOSFETs are similar. CNFETs benefit from a unique one-dimensional band structure that suppresses backscattering and makes near-ballistic operations [23]. Therefore, their switching speed is higher than MOSFETs. In term of power consumption, due to low off-current, CNFETs consume less power than MOSFETs [22]. Another remarkable attribute of CNFETs is that by changing the diameter of nanotubes, their threshold voltage can be altered. As a result, these transistors are well-suited for multi-threshold designs [16]. Manufacturing of CNFETs involves some difficulties such as non-perfect growth of carbon nanotubes [24], the inaccurate diameter of CNTs [25], and inaccurate alignment of the CNTs under the same gate of the CNFET [26]. Despite these obstacles, it is worth noting that recently researchers have successfully fabricated a 16-bit microprocessor based on CNFET technology which is a breakthrough in designing digital circuits [27].

Considering the remarkable advantages of the CNFET technology, we present a high-speed and low-energy 1-bit approximate full adder cell in this paper. The proposed design uses both pass transistor logic (PTL) and transmission gate logic (TGL) styles to improve transistor-level figures of merit. To further reduce power consumption, we have altered the standard truth table of the full adder cell to diminish the switching activity of output signals (i.e., SUM and output carry) while keeping the produced error to a minimum as much as possible. In other words, we take into account both switching and application levels of abstraction to enhance hardware criteria at the cost of producing some errors at the outputs. The proposed design is compared with some state-of-the-art designs from a diverse range of aspects. At the switching level, circuits are investigated in terms of power, delay, power-delay product (PDP), energy-delay product (EDP), and power-delay-area product (PDAP) in various power supplies, temperatures, and output loads. The effects of diameter variations of CNTs as one of the major constraints of the CNFET technology on the performance of the proposed cell is scrutinized by Monte Carlo (MC) transient analysis. At the application level, all circuits under study are applied to image blending application of image processing to study their efficiency regarding peak signal-to-noise ratio (PSNR) and structural similarity (SSIM) index criteria. Moreover, to have a fair comparison we investigate circuits using a figure of merit

that simultaneously takes into account both hardware and application level evaluations metrics. The simulation results confirm that the proposed cell shows a significant improvement over the previous designs in terms of latency and energy consumption parameters.

The remainder of this paper is organized as follows. In Section 2, the CNFET technology and approximate computing are briefly reviewed. In Section 3, the analysis of several state-of-the-art inaccurate full adders is provided in detail. In this section, transistor-level metrics and error analysis for each cell are provided. The novel approximate full adder design is presented in detail in Section 4. Section 5, provides computer simulations and discussions. Finally, conclusions are provided in Section 6.

2. Background

2.1. CNFET technology

Carbon nanotubes (CNTs) are hollow cylinders of graphite that were first discovered by Sumio Iijima in 1991 [28]. They contained several nested nanotubes and hence were called multi-walled carbon nanotubes (MWCNTs). Then, single-walled carbon nanotubes (SWCNTs) were discovered in 1993 which are suitable for designing digital electronic circuits [29,30]. By rolling up a one-atom-thick sheet of graphene, tubular SWCNTs are formed. The rolling-up direction which is called Chiral vector determines the electrical properties of the nanotubes. The Chiral vector, as shown in Eq. (1), consists of two unit vectors namely \vec{a}_1 and \vec{a}_2 , and two integer numbers m and n [30]. If $m = n$ or $|m - n| = 3k$ (k is an integer number) then CNT is metallic, and otherwise, it functions as a semiconductor substance.

$$\vec{C} = m\vec{a}_1 + n\vec{a}_2 \quad (1)$$

The diameter of a CNT is obtained by Eq. (2) [31].

$$D_{CNT} = \frac{\sqrt{3}\alpha_0(m^2 + n^2 + mn)^{1/2}}{\pi} \simeq 0.0783 \times (m^2 + n^2 + mn)^{1/2} \quad (2)$$

Where $\alpha_0 = 0.142$ nm is the distance of two neighboring carbon atoms. The SWCNTs are used as the channel of CNFET devices. The threshold voltage of a CNFET (V_{th}) is obtained using Eq. (3) [32].

$$V_{th} = \frac{\alpha' V_{\pi}}{\sqrt{3}eD_{CNT}} = \frac{\sqrt{3}\alpha_0 V_{\pi}}{\sqrt{3}eD_{CNT}} \simeq \frac{0.43}{D_{CNT}} \quad (3)$$

Where V_{π} , $\alpha' = \sqrt{3}\alpha_0 = 0.249$ nm, and e stand for carbon π - π CNTs bond energy in the tight-binding model ($\simeq 3.033$ eV), the lattice constant, and the charge value of a single electron, respectively. Schottky barrier and MOSFET-like are two kinds of CNFETs that are being extensively studied. MOSFET-like transistors have significant properties such as lower OFF leakage current and higher ON current than Schottky barrier transistors [33]. Therefore, in this paper, all circuits are simulated using the MOSFET-like CNFET model.

2.2. Error analysis metrics

Humans receive approximately 75 % of the information through the sense of eyesight [34]. On the other hand, many digital systems are designed to interface with humans [6]. Humans have limited perceptual capacity in the interpretation of images, videos, and sounds. Therefore, approximate computing can trade accuracy with circuit parameters such as power, delay, area, PDP, and EDP. Table 1 shows the key error metrics that are used to judge approximate cells concerning accuracy in this paper [7]. Error distance (ED) is the difference between exact output (S) and inexact output (S') for each input combination. Maximum error distance (MAE) is the maximum value of ED. Total error distance (TED) is obtained by summation of all EDs. Symbol N denotes the number of input combinations. For instance, a full adder cell has three inputs, and

Table 1

Error metrics with their brief explanations.

Error Metric	Description	Equation	Equation No.
ED	Error distance	$ S - S' $	(4)
MAE	Maximum error distance	$Maximum (ED)$	(5)
TED	Total error distance	$\sum_{i=1}^N ED_i$	(6)
MED	Mean error distance	$MED = \frac{TED}{N}$	(7)
NED	Normalized mean error distance	$NED = \frac{MED}{Max}$	(8)

the value of N is eight. Mean error distance (MED) is obtained by computing the average value of TED. Finally, normalized mean error distance (NED) which is independent of bit-width is obtained by dividing MED by the maximum value that a circuit can produce. It is worth noting that for a circuit with n -bit width the maximum output is $2^{n+1}-1$.

2.3. Switching activity

Power consumption in digital circuits consists of three main components, i.e. dynamic, static, and short-circuit. The total power consumption is shown in Eq. (9).

$$P_{Total} = P_{Dynamic} + P_{Static} + P_{Short-circuit}$$

$$= fV_{DD}^2 \sum_{i=1}^n \alpha_i C_i + V_{DD} \sum_{i=1}^n I_{L,i} + V_{DD} \sum_{i=1}^n I_{SC,i} \quad (9)$$

Where f , α , C , I_L , I_{SC} , and n stand for operating frequency, switching activity, node capacitance, leakage current, short-circuit current, and the number of nodes, respectively. Among these components, dynamic power has the highest contribution to the total power consumption of a digital circuit [35]. According to Eq. (9), dynamic power consumption can be reduced by decreasing the switching activity parameter. In approximate circuits, switching activity can be reduced in return for some error generation. The switching activity of a node in a full adder cell is computed by Eq. (10).

$$Switching \ activity (\alpha) = \frac{Number \ of \ '0s'}{8} \times \frac{Number \ of \ '1s'}{8} \quad (10)$$

Since output nodes of full adder cells are often driving external large loads, it is an essential task to calculate and analyze their switching activity. In this regard, first, the switching activity of SUM (α_{SUM}) and output carry (α_{Cout}) are calculated separately. Then, the switching activity of the full adder cell (α_{cell}) is approximated by adding the switching activity of SUM and Cout nodes.

3. Literature review

The structure of an approximate full adder cell which is called VAXA is shown in Fig. 1 [36]. It includes eight transistors, three of which are on

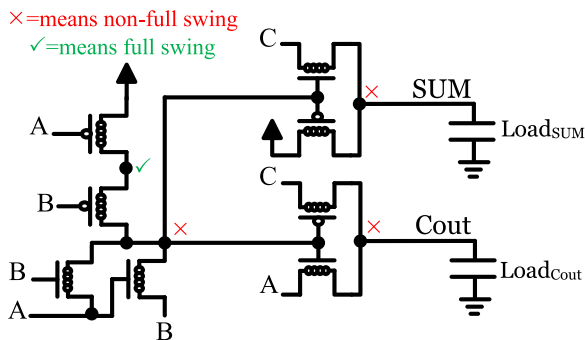


Fig. 1. The VAXA design [36].

the critical delay path. None of the internal and external nodes in this circuit is full voltage swing. In Fig. 1, the full and non-full voltage swing nodes are demonstrated with the cross (i.e., 'x') and tick (i.e., '✓') marks, respectively. Non-full voltage swing nodes result in weak output signals. This handicap increases both latency and power consumption due to a lowering slope in the transition region. This circuit has a low transistor count at the cost of weak outputs. The switching activity of Cout, SUM, and cell are 0.25, 0.1875, and 0.4375, respectively. The SUM output is erroneous in two cases while the Cout output is true for all possible combinations of inputs. The MED and NED metrics of VAXA are 0.25 and 0.0833, respectively.

Fig. 2 illustrates the schematic of the NNIFA approximate full adder cell [37]. The NNIFA includes twelve transistors, four of which are placed on the critical delay path. The existence of a non-full voltage swing common node to produce SUM and Cout signals is another major problem of this design. Besides, the SUM output is not rail-to-rail. Moreover, the common node is connected to the LoadSUM and two gate terminals of the inverter gate. In other words, it has to drive a large load. Therefore, the inverter gate which is used to generate the Cout signal will switch slowly, leading to a significant increase in circuit latency. The switching activity of Cout, SUM, and cell are 0.25, 0.25, and 0.5, respectively. The high switching activity of the NNIFA design causes higher power consumption. The SUM signal is incorrect in two cases while the Cout signal is correct. The MED and NED metrics of the NNIFA cell are 0.25 and 0.0833, respectively.

The transistor-level implementation of the 9TIFA design which is based on capacitive threshold logic (CTL) is shown in Fig. 3 [38]. The 9TIFA consists of nine transistors, three of which are placed on the critical delay path. The SUM signal is not a full voltage swing output. Furthermore, the capacitive network produces a signal which is not full voltage swing when the summation of inputs is 1 or 2. Therefore, it makes the inverter gate, which is connected to this weak node, have a lower switching speed and higher power consumption. Therefore, the latency and power consumption of the 9TIFA design will be high. The switching activity of the 9TIFA for Cout, SUM, and cell is 0.25, 0.1093, and 0.3593, respectively. In this design, the Cout signal is correct while the SUM signal is erroneous in three cases. From an accuracy point of view, the MED and NED metrics are 0.375 and 0.125, respectively.

Fig. 4 depicts the structure of the BBIFA design which is based on bridge logic style [39]. It contains twelve transistors, four of which are placed on the critical delay path. Output signals are full voltage swing. Similar to the NNIFA design, the significant drawback of this design is that it shares a common node to produce the SUM and Cout signals. As mentioned before, the common node which is driving LoadSUM is connected to the input of the inverter gate. Accordingly, the inverter gate, which is responsible for generating output carry, switches at a slower rate, leading to increased latency and even power consumption. The switching activity of Cout, SUM, and cell is 0.25, 0.25, and 0.5, respectively. The Cout signal is correct for all possible combinations of inputs while the SUM signal produces two erroneous outputs. The MED and NED accuracy metrics are 0.25 and 0.0833, respectively.

The structure of the AFA1 design which is based on standard CMOS (S-CMOS) logic style is demonstrated in Fig. 5 [40]. It is constructed using only eight transistors, three of which are placed on the critical delay path. As depicted in Fig. 5, all internal and external nodes in the AFA1 cell are rail-to-rail. According to the structure of the AFA1 design, the critical delay path is from the inputs to the output of the Cout. There is a common node that is used to generate output signals. Since the common node does not have sufficient strength to drive LoadSUM and inverter gate at the same time, the delay of the AFA1 is significantly increased. The switching activity of Cout, SUM, and cell are 0.2343, 0.2343, and 0.4686, respectively. Low transistor count and switching activity result in lower power consumption. The SUM and Cout outputs have three and one errors, respectively. The AFA1 circuit propagates error to higher significant positions and results in larger computational errors. The MED and NED are 0.375 and 0.125, respectively. Therefore,

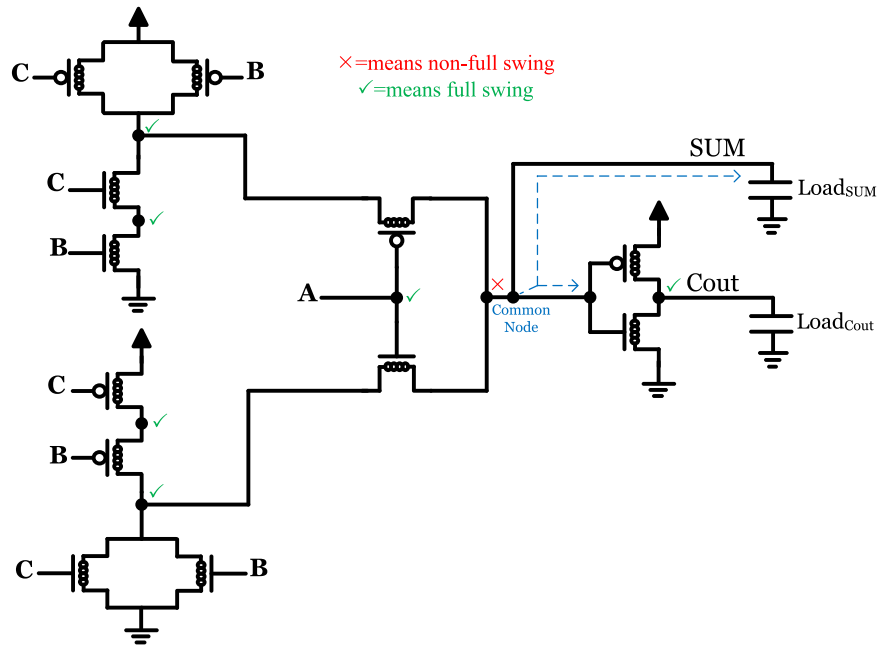


Fig. 2. The NNIFA design [37].

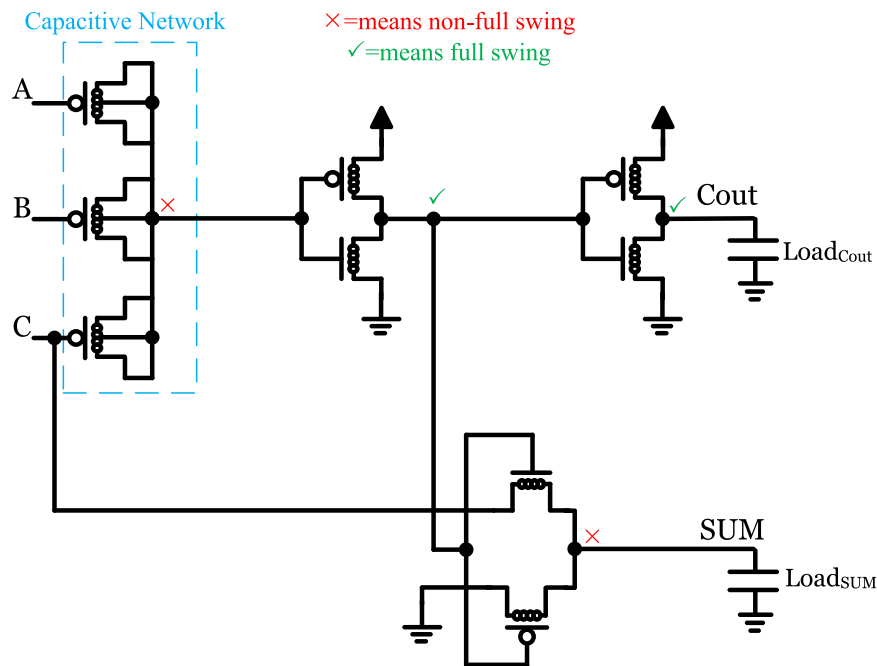


Fig. 3. The 9TIFA design [38].

although this design improves the power consumption parameter, it leads to producing large errors.

The structure of the 9TIFA2 approximate full adder cell which is based on CMOS logic style is shown in Fig. 6 [41]. This design includes nine transistors, three of which are on the critical delay path. All nodes in the structure of the 9TIFA2 are rail-to-rail. Similar to the NNIFA, BBIFA, and AFA1 designs, the 9TIFA2 cell uses a common node to produce output signals, i.e. SUM, and Cout. Therefore, the 9TIFA2 is expected to have a long propagation delay. The switching activity of Cout, SUM, and cell is 0.2343, 0.2343, and 0.4686, respectively. Low transistor count and switching activity result in the reduction of power consumption. The 9TIFA2 produces erroneous outputs for SUM and Cout signals similar to that of the AFA1 design. The MED and NED for the

9TIFA2 design are 0.375 and 0.125, respectively.

Fig. 7 shows an approximate full adder cell based on the CTL logic which is called 15TIFA2 [42]. This design consists of fifteen transistors, four of which are placed on the critical delay path. The switching activity of Cout, SUM, and cell is 0.25, 0.2343, and 0.4843, respectively. There are two capacitive networks in the structure of the 15TIFA2. These networks produce non-full swing internal signals that incur more power consumption and slower switching speed of consecutive transistors. The SUM signal is erroneous in three cases but the Cout signal is true for all combinations of inputs. The MED and NED values are 0.375 and 0.125, respectively.

The structure of the APA2 approximate full adder cell is depicted in Fig. 8 [43]. It is based on both CMOS and transmission gate logic styles.

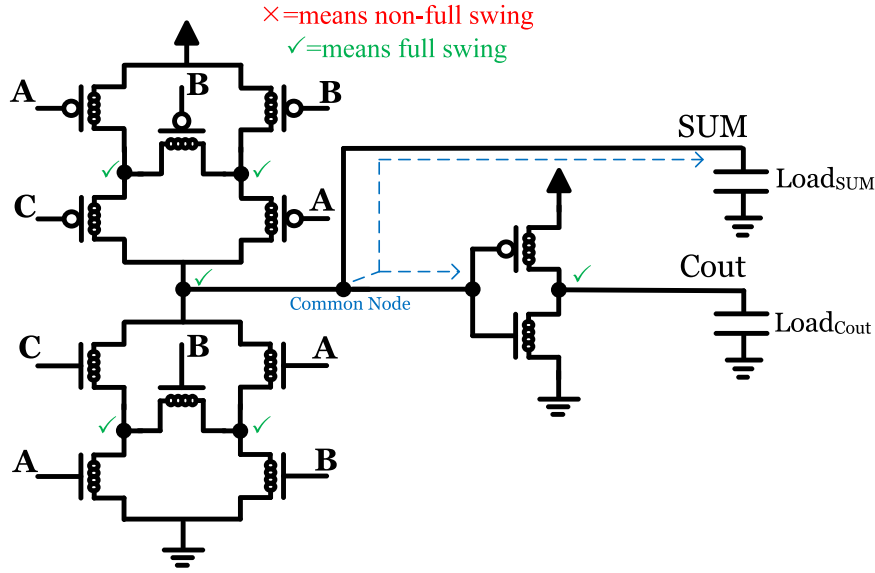


Fig. 4. The BBIFA design [39].

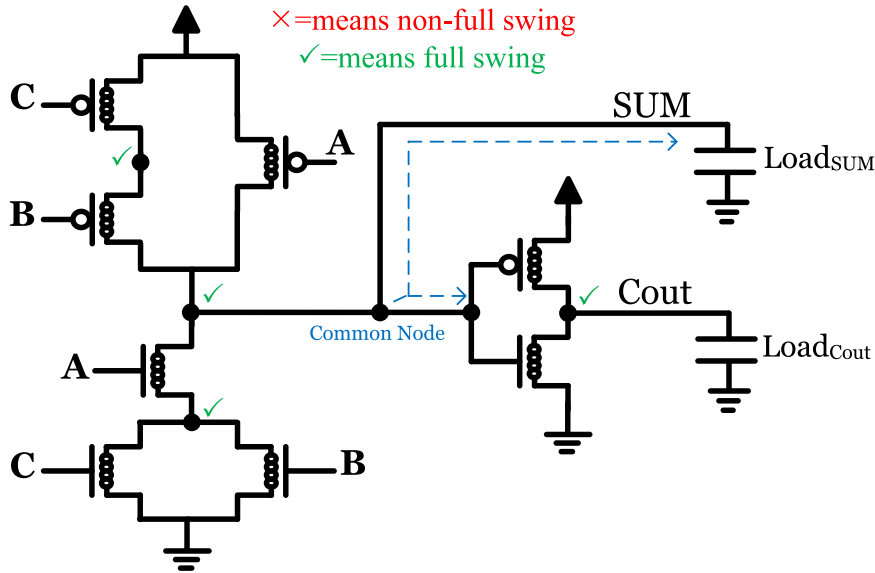


Fig. 5. The AFA1 design [40].

It includes sixteen transistors, five of which are on the critical delay path. All internal and external nodes of the APA2 design are rail-to-rail. Although this circuit has a common node, since it is fed directly by a strong input signal, it will not have much negative effect on the delay of the circuit. The switching activity of Cout, SUM, and cell is 0.25, 0.25, and 0.5, respectively. From an accuracy point of view, both outputs are incorrect in two cases. The MED and NED criteria are 0.75 and 0.25, respectively, which are almost high.

Table 2 compares the efficiency of state-of-the-art approximate full adders in terms of circuit and accuracy points of view. In Table 2, symbols “F. S.,” “C. N.,” and “C. P.” denote “Full Swing,” “Common Node,” and “Critical Path,” respectively. Among the cells under study, only the VAXA, NNIFA, and 9TIFA designs do not have full voltage swing outputs. All designs except for the VAXA, 9TIFA, and 15TIFA2 have common node obstacles that negatively affect latency and power consumption metrics. The APA2 design consists of the highest number of transistors. On the other hand, the VAXA and AFA1 have the lowest transistor count. From an accuracy point of view, the VAXA, NNIFA, and

BBIFA designs have the lowest NED, but the APA2 design has the highest NED.

4. Proposed approximate full adder

In this section, the design and analysis of a novel high-speed and low-energy approximate full adder cell are presented in detail. The proposed cell is obtained using Eqs. (11) and (12).

$$Cout(A, B, C) = A'.0 + A.(B + C) \quad (11)$$

$$SUM(A, B, C) = A'.1 + A.(B.C) \quad (12)$$

The proposed design uses 2-input AND and OR functions to produce SUM and Cout outputs. A symmetric structure based on pass transistor logic and transmission gate logic is used to implement the novel approximate full adder circuit. Therefore, the proposed cell can be called as pass transistor and transmission gate based approximate full adder cell (PTAFA). The 2-to-1 multiplexers that are used to produce output

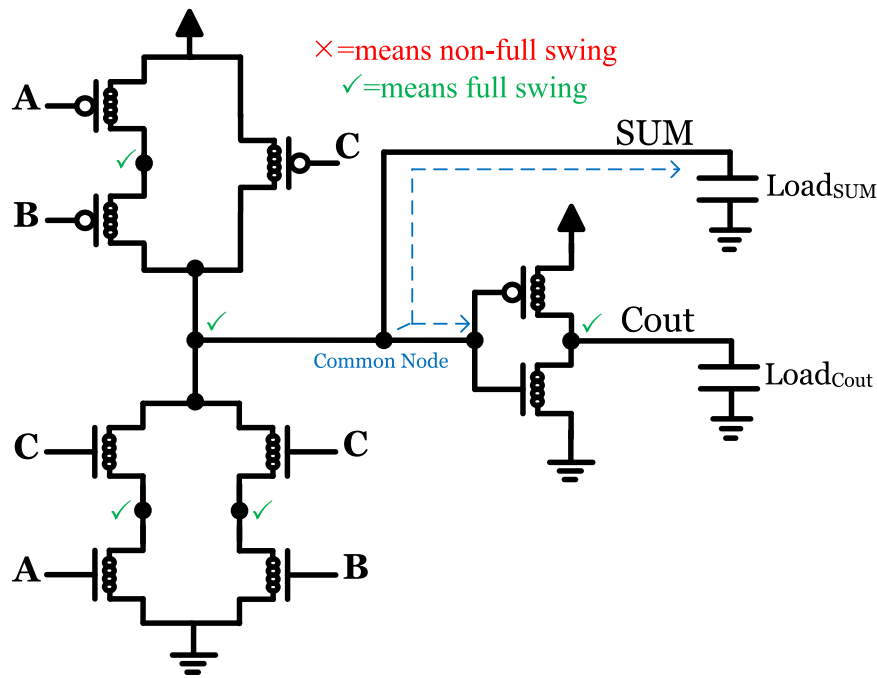


Fig. 6. The 9TIFA2 design [41].

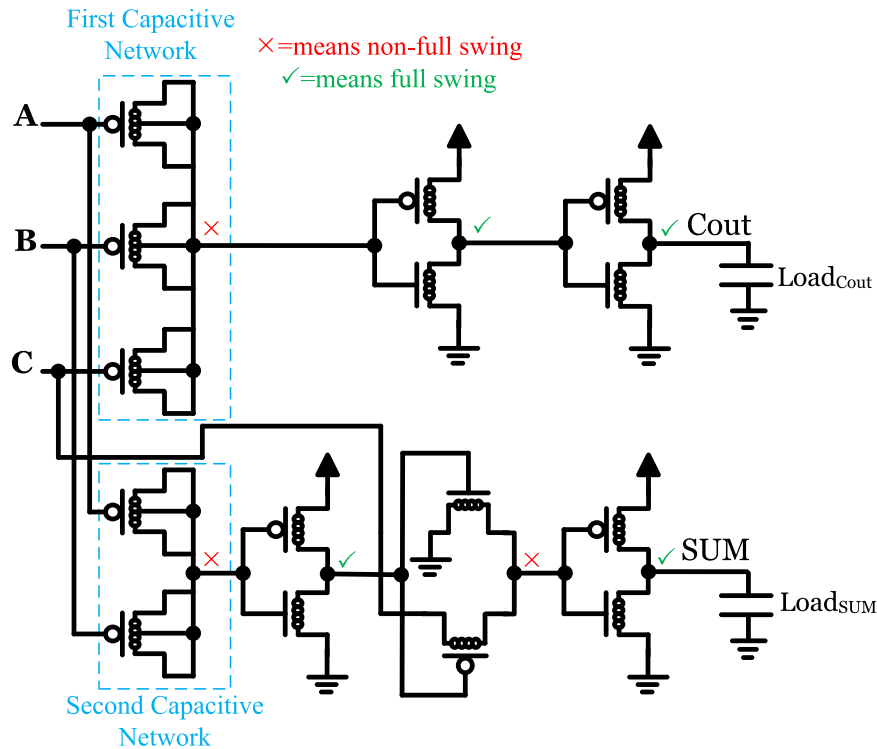


Fig. 7. The 15TIFA2 design [42].

signals are realized by the combination of PTL and TGL circuits. Therefore, they are implemented with only three transistors. They use input 'A' as their select line. The schematic of the proposed PTFAFA design which is composed of sixteen transistors is indicated in Fig. 9.

The existence of PTL and TGL circuits results in a reduction of power consumption due to the elimination of the direct path between the power supply (V_{DD}) and ground (GND) terminals. Transmission gate logic always provides full voltage swing outputs. Contrary to TGL, although the PTL based circuits do not guarantee rail-to-rail outputs, it

has been used in the proposed design in such a way that the outputs are full voltage swing. As depicted in Fig. 9, all internal and external nodes of the proposed cell are in full swing state which leads to the faster-switching operation of transistors and consequently lower power consumption. Unlike the previous NNIFA, BBIFA, AFA1, 9TIFA2, and APA2, the proposed PTFAFA design does not use a weak common node to produce both SUM and Cout output signals. We already mentioned that a common node can negatively affect circuit figures of merit. Some previous designs have sacrificed the efficiency parameters in exchange for

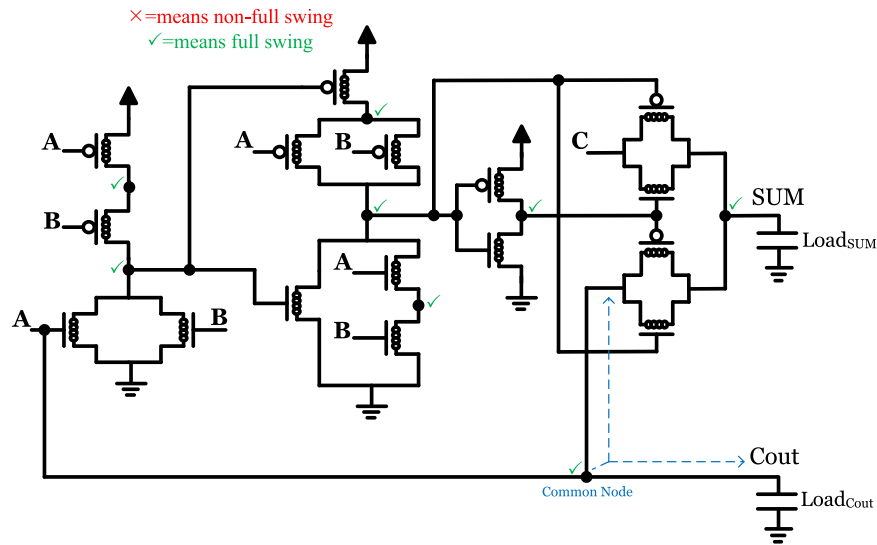


Fig. 8. The APA2 design [43].

Table 2
Attributes of approximate full adder cells.

Design	VAXA	NNIFA	9TIFA	BBIFA	AFA1	9TIFA2	15TIFA2	APA2
Ref. No.	[36]	[37]	[38]	[39]	[40]	[41]	[42]	[43]
Truth Table								
Inputs	Outputs							
a b c	Cout	SUM	Cout	SUM	Cout	SUM	Cout	SUM
0 0 0	0	0	0	× 1	0	0	0	0
0 0 1	0	1	0	1	0	1	0	1
0 1 0	0	1	0	1	0	1	0	1
0 1 1	1	× 1	1	0	1	0	1	0
1 0 0	0	1	0	1	0	1	0	1
1 0 1	1	× 1	1	0	1	0	1	0
1 1 0	1	0	1	0	1	0	1	0
1 1 1	1	1	1	× 0	1	× 0	1	1
Circuit Metrics								
F. S.	No	No	Yes	No	Yes	No	Yes	Yes
C. N.	No	Yes	No	Yes	Yes	Yes	No	Yes
C. P.	3	4	3	4	3	3	4	5
Tr. No.	8	12	9	12	8	9	15	16
α_{Cout}	0.25	0.25	0.25	0.25	0.2343	0.2343	0.25	0.25
α_{SUM}	0.1875	0.25	0.1093	0.25	0.2343	0.2343	0.2343	0.25
α_{Cell}	0.4375	0.5	0.3593	0.5	0.4686	0.4686	0.4843	0.5
Accuracy Metrics								
Error	0	2	0	2	0	3	0	3
MAE	1	1	1	1	1	1	1	2
TED	2	2	3	2	3	3	3	6
MED	0.25	0.25	0.375	0.25	0.375	0.375	0.375	0.75
NED	0.0833	0.0833	0.125	0.0833	0.125	0.125	0.125	0.25

reducing the number of transistors, which is not reasonable. Since there is no threshold loss problem within the proposed cell, the diameter of all CNTs (D_{CNT}) is set to 1.4877 nm which is standard at the 32 nm CNFET technology node. Hence, using Eq. (3), the threshold voltage of all transistors is 0.28 V. Moreover, the number of tubes is three for all CNFETs. The critical delay path of the PTFAFA cell consists of three transistors. Table 3, shows the truth table and figures of merit for the proposed cell at both circuit and accuracy levels of abstraction. As shown in Table 3, the proposed cell provides erroneous outputs for both Cout and SUM signals. The Cout and SUM signals are faulty in one and three cases, respectively. The switching activity of Cout, SUM, and cell is 0.2343, 0.2343, and 0.4686, respectively. The switching activity of the proposed PTFAFA design is equal to the AFA1 and 9TIFA2 designs and less than the NNIFA, BBIFA, 15TIFA2, and APA2 designs. From an accuracy point of view, its MED and NED error metrics are 0.375 and 0.125, respectively.

Fig. 10 illustrates the input and output waveforms snapshot of the proposed PTFAFA approximate full adder cell at the presence of all possible combinations of inputs. Simulation is carried out in 0.9 V power supply, room temperature of 25 °C, fanout of four inverter gates at each output node, and 1 GHz operating frequency. As shown in Fig. 10, the outputs of the proposed cell do not produce any spike or glitch and are in accordance with the truth table of the circuit. Therefore, the proposed cell can be effectively applied in digital electronic systems.

5. Simulation results and discussion

5.1. Switching level

Simulations using the HSPICE tool are carried out to evaluate various designs. The efficiency of the circuits under test in terms of various figures of merit including power consumption, delay, power-delay

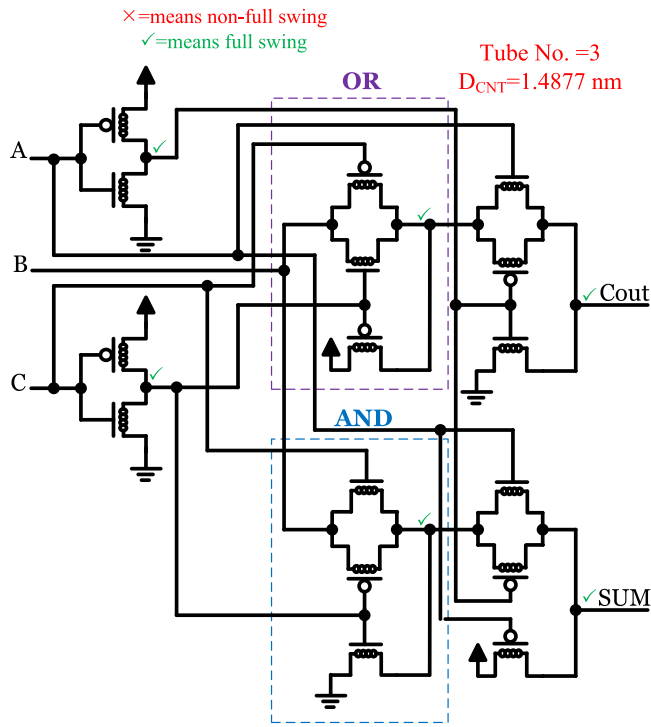


Fig. 9. The schematic of the proposed PTFA design.

product, energy-delay product, and power-delay-area product is studied at diverse conditions. For simulations, the compact SPICE model which is developed at Stanford University for unipolar MOSFET-like CNFETs is used [44,45]. The CNFET library model is for 32 nm channel length and includes non-idealities such as Schottky barrier, CNT charge screening, and parasitic effects including CNT, source/drain, and gate resistances and capacitances. Table 4 describes key parameters of the CNFET model with their brief explanations.

Fig. 11 clarifies the simulation environment for circuits under test (CUT) [46]. Buffers are applied at the input nodes to simulate input signals with spikes and enough distortions as expected in a real environment. To assess the efficiency of the circuits precisely, an exhaustive

test with 56 input patterns is carried out. At the output nodes, a standard fanout of four (FO4) inverter gates is used. The delay metric is measured from the moment that the input signal reaches 50 % of its final value until the output signal reaches the same point. This measurement is done for all transitions at the output nodes of SUM and Cout. At last, the largest value is reported as the delay of the circuit. Average power consumption is measured during a long period for all components existing in Fig. 11. Power-delay product and energy-delay product are taken into account as two important criteria. They make a trade-off between power dissipation and delay, and are fair metrics to evaluate the efficiency of circuits. The tube diameter and number are set to 1.4877 nm and 3, respectively. Hence, considering Eq. (3), the threshold voltage of each transistor will be 0.289 V. For transistors that have a threshold loss problem, the diameter of the tubes is set to 5.7159 nm. Therefore, the threshold voltage will be 0.0752 V, and the minimum voltage loss is obtained at the output of these transistors.

Table 5 indicates simulation results of circuits with regard to diverse power supplies (i.e., V_{DD}) at 1 GHz operating frequency, FO4 load, and room temperature of 25 °C. The nominal power supply for the 32 nm CNFET technology node is 0.9 V. In this simulation, we scale the power supply to 0.8 V and 1 V to examine the robustness of the circuits against V_{DD} variations. As depicted in Table 5, circuit-level metrics including power dissipation, delay, PDP, EDP, and PDAP are taken into account. From a power dissipation point of view, the 9TIFA and 15TIFA2 designs have the worst operation because using capacitive threshold logic which provides non-full voltage swing internal signals. The AFA1 and 9TIFA2 designs have the least amount of power consumption than others due to featuring low transistor count and full voltage swing outputs. The VAXA, NNIFA, BBIFA, and APA2 designs have about equal power consumption. Their power consumption is more than the AFA1 and 9TIFA2 designs. Although the VAXA has only eight transistors it consumes more power because its SUM and Cout outputs are not rail-to-rail. The reason for higher power consumption for the NNIFA, BBIFA, and APA2 circuits is that they have a high number of transistors and a common node (defined in Section 3) for generating output signals. It is worth noting that the proposed PTFA cell has the lowest power consumption after the AFA1 and 9TIFA2 designs. Because it has full voltage swing outputs and does not have a common node. Generally, there is close competition between circuits under investigation from a power consumption point of view.

Simulation results indicate that the lowest delay belongs to the proposed PTFA design due to its remarkable characteristics such as

Table 3
Attributes of the proposed full adder cell.

Inputs			Internal functions		Exact outputs		Inexact outputs		Error distance	
A	B	C	OR (B, C)	AND (B, C)	Cout	SUM	Cout	SUM		
0	0	0	0	0	0	0	0	× 1	1	
0	0	1	1	0	0	1	0	1	0	
0	1	0	1	0	0	1	0	1	0	
0	1	1	1	1	1	0	× 0	× 1	1	
1	0	0	0	0	0	1	0	× 0	1	
1	0	1	1	0	1	0	1	0	0	
1	1	0	1	0	1	0	1	0	0	
1	1	1	1	1	1	1	1	1	0	
Circuit Metrics										
Full Swing (Cout)			Full Swing (SUM)		Critical Path	C. N.	Tr. No.	α _{Cout}	α _{SUM}	α _{Cell}
Yes			Yes		3	No	16	0.2343	0.2343	0.4686
Accuracy Metrics										
Errors in Cout			Errors in SUM		TED		MAE	MED		NED
1			3		3		1	0.375		0.125

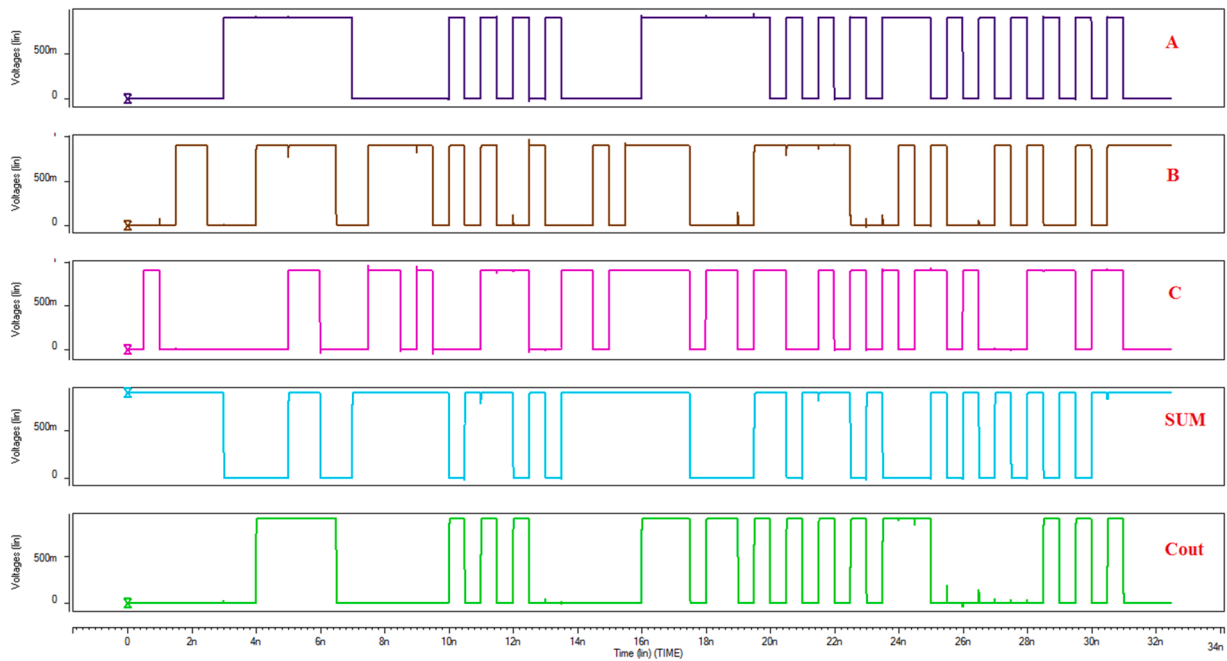


Fig. 10. The snapshot of the waveforms of the proposed design.

Table 4

Key parameters of the CNFET model [44,45].

Parameter	Value	Brief description
L_{ch}	32 nm	Physical channel length
L_{geff}	100 nm	The mean free path in the intrinsic CNT channel
L_{ss}	32 nm	The length of the doped CNT source-side extension region
L_{dd}	32 nm	The length of the doped CNT drain-side extension region
K_{gate}	16	The dielectric constant of high-K top gate dielectric material
T_{ox}	4 nm	The thickness of high-K top gate dielectric material
C_{sub}	40 pF/m	The coupling capacitance between the channel region and the substrate
E_{fi}	0.6 eV	The Fermi level of the doped S/D tube
Pitch	16 nm	The distance between the centers of two neighboring CNTs under the same gate
Tubes	3	The number of carbon nanotubes for each CNFET
(m, n)	(19, 0)	The chirality integer pair of each carbon nanotube

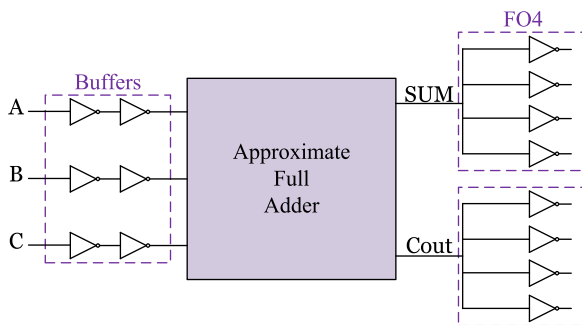


Fig. 11. Simulation environment [46].

short critical path, rail-to-rail signals at both internal and output nodes, and not having a common node. For instance, at 0.9 V V_{DD} , the proposed cell offers 27.9 %, 41.1 %, 17.9 %, 51.4 %, 33 %, 41.9 %, 22.6% and 20.8 % less delay compared to the VAXA, NNIFA, 9TIFA, BBIFA, AFA1, 9TIFA2, 15TIFA2, and APA2 designs, respectively. Since the proposed PTAFA design has low power consumption and delay, it outperforms other designs in terms of PDP and EDP figures of merit. For instance, at

1 V V_{DD} , it remarkably improves the EDP metric about 34 %, 73 %, 86 %, 80 %, 58 %, 71 %, 86% and 50 % compared to the VAXA, NNIFA, 9TIFA, BBIFA, AFA1, 9TIFA2, 15TIFA2, and APA2 designs, respectively. From the PDAP point of view, the proposed design has better performance after the AFA1, VAXA, and 9TIFA2 designs. Considering simulation results, the proposed design not only is robust versus power supply variations but also provides superior results compared to its counterparts.

Robustness of 9TIFA2, 15TIFA2, APA2, and the proposed PTAFA cells is studied in the presence of supply voltage (V_{DD}) reduction. Simulation results are presented in Table 6. The 15TIFA2 cannot work with voltages lower than 0.5 V. But the other cells work properly at a minimum supply voltage of 0.3 V. The lowest delay, PDP, and EDP belong to the proposed PTAFA design. Therefore, the proposed cell can be efficiently used in low-power applications.

Stability and keeping the proper performance of circuits against changes in ambient temperatures have always been of particular importance. Circuits have to be resistant to temperature variations. To examine the robustness of circuits, they are simulated in 0.9 V V_{DD} , 1 GHz operating frequency, the load of FO4, and various temperatures ranging from 0 °C to 60 °C. As shown in Fig. 12, the lowest delay and PDP belong to the proposed approximate full adder cell. The slope of changes in power consumption, latency, and the energy consumption is almost constant which shows that the proposed circuit has a good performance against different temperatures.

The performance metrics of the all approximate full adder cells are assessed against a wide range of loads from FO1 to FO8 at 0.9 V power supply, 1 GHz operating frequency, and room temperature. Simulation results are illustrated in Fig. 13. Considering Fig. 13, it is evident that the proposed cell has the least delay and PDP compared to its counterparts. Therefore, it can be effectively used in the structure of larger arithmetic circuits. The worst PDP belongs to the 15TIFA2, 9TIFA, and BBIFA, respectively.

The high-precision fabrication of carbon nanotubes is one of the difficulties of CNFET technology [25]. It is always likely for the diameter of the nanotubes to differ from the values specified by the circuit designer. According to Eq. (3), the diameter of the nanotube affects the threshold voltage of the CNFET device. Therefore, the diameter variation can negatively affect the circuit performance. In this section, we

Table 5
Simulation results of power supply scaling.

Design	Power (10 ⁻⁶ W)	Delay (10 ⁻¹² S)	PDP (10 ⁻¹⁷ J)	EDP (10 ⁻²⁹ J.S)	Tr. No.	PDAP (10 ⁻¹⁷ J)
Vdd= 1 V						
VAXA	1.6648	11.432	1.9033	21.7585	8	15.2264
NNIFA	1.6326	18.261	2.9812	54.4396	12	35.7744
9TIFA	5.6500	13.640	7.7068	105.120	9	69.3612
BBIFA	1.5892	21.572	3.4283	73.9552	12	41.1396
AFA1	1.3531	15.943	2.1572	34.3922	8	17.2576
9TIFA2	1.3726	18.951	2.6013	49.2972	9	23.4117
15TIFA2	5.9624	13.223	7.8839	104.248	15	118.258
APA2	1.6803	13.061	2.1946	28.6636	16	35.1136
PTAFA[Proposed]	1.5387	9.6363	1.4827	14.2877	16	23.7232
Vdd= 0.9 V						
VAXA	1.1997	15.623	1.8742	29.2806	8	14.9936
NNIFA	1.1671	19.132	2.2329	42.7198	12	26.7948
9TIFA	3.2707	13.725	4.4891	61.6128	9	40.4019
BBIFA	1.1118	23.207	2.5801	59.8763	12	30.9612
AFA1	0.94111	16.814	1.5824	26.6064	8	12.6592
9TIFA2	0.96632	19.395	1.8742	36.3501	9	16.8678
15TIFA2	3.4730	14.550	5.0531	73.5226	15	75.7965
APA2	1.1984	14.216	1.7036	24.2183	16	27.2576
PTAFA[Proposed]	1.0779	11.258	1.2134	13.6604	16	19.4144
Vdd= 0.8 V						
VAXA	0.83970	16.466	1.3826	22.7658	8	11.0608
NNIFA	0.76038	20.727	1.5761	32.6678	12	18.9132
9TIFA	1.7022	14.066	2.3943	33.6782	9	21.5487
BBIFA	0.71857	24.719	1.7762	43.9058	12	21.3144
AFA1	0.57532	18.183	1.0461	19.0212	8	8.3688
9TIFA2	0.63280	20.929	1.3244	27.7183	9	11.9196
15TIFA2	1.9724	15.706	3.0978	48.6540	15	46.467
APA2	0.80403	15.603	1.2545	19.5739	16	20.072
PTAFA[Proposed]	0.67657	11.934	0.80743	9.63586	16	12.9188

Table 6
Simulation results in minimum supply voltage.

Design	Ref.	Minimum V _{DD} (V)	Power (10 ⁻⁸ W)	Delay (10 ⁻¹² S)	PDP (10 ⁻¹⁹ J)	EDP (10 ⁻³¹ J.S)
9TIFA2	[41]	0.3	3.0351	94.015	28.535	2682.71
15TIFA2	[42]	0.5	54.613	270.32	1476.3	39,9073.4
APA2	[43]	0.3	4.0270	86.323	34.762	3000.76
PTAFA	[Proposed]	0.3	3.6959	65.402	24.172	1580.89

examine the degree of resistance of the proposed PTAFA approximate full adder cell to the diameter variations of carbon nanotubes using the Monte Carlo (MC) transient analysis [22]. In Monte Carlo analysis, each simulation cycle is repeated 30 times. The importance of 30 repetitions is very high. If a circuit operates correctly in all 30 iterations, there is a 99 % probability that more than 80 % of the circuit components will work properly [47]. To model the diameter variations of CNTs, the *Gaussian* function with the distribution of 6-Sigma is employed. To examine the resistance of the proposed cell concerning diameter variations of CNTs, a standard deviation from the mean diameter value in the range of 0.05–0.2 nm is considered [48]. As shown in Eqs. (13), (14), and (15), the mean (μ), variance (σ^2), and standard deviation (σ) are taken into account.

$$\mu = \frac{x_1 + x_2 + \dots + x_n}{N} \quad (13)$$

$$\sigma^2 = \frac{(x_1 - \mu)^2 + (x_2 - \mu)^2 + \dots + (x_n - \mu)^2}{N - 1} \quad (14)$$

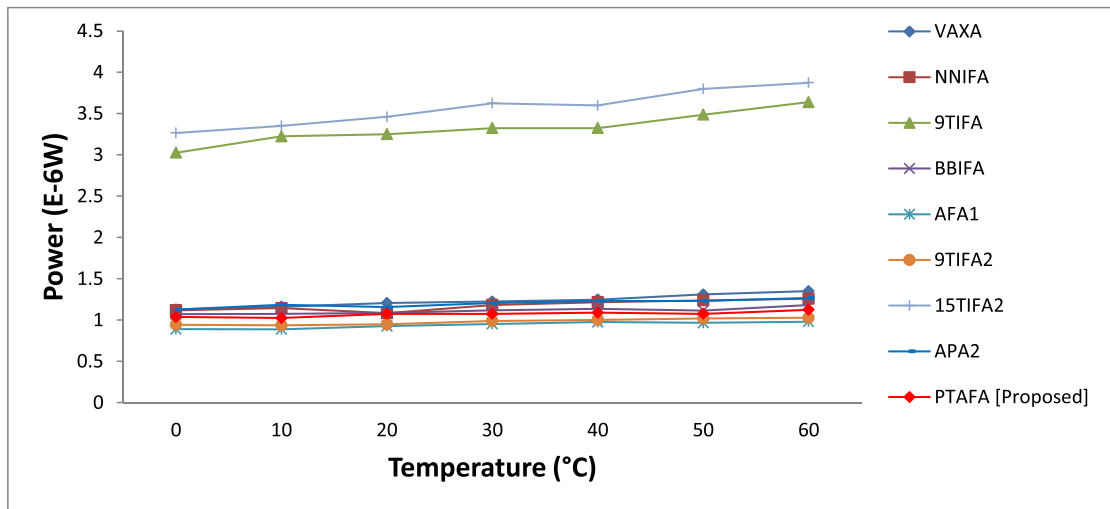
$$\sigma = \sqrt{\sigma^2} \quad (15)$$

Where symbols x_i and N stand for the value of each variable and the number of variables, respectively. As mentioned earlier, we consider $N = 30$ in this simulation. Simulation results are shown in Table 7. These results confirm that the proposed cell is robust against the diameter variations of CNTs.

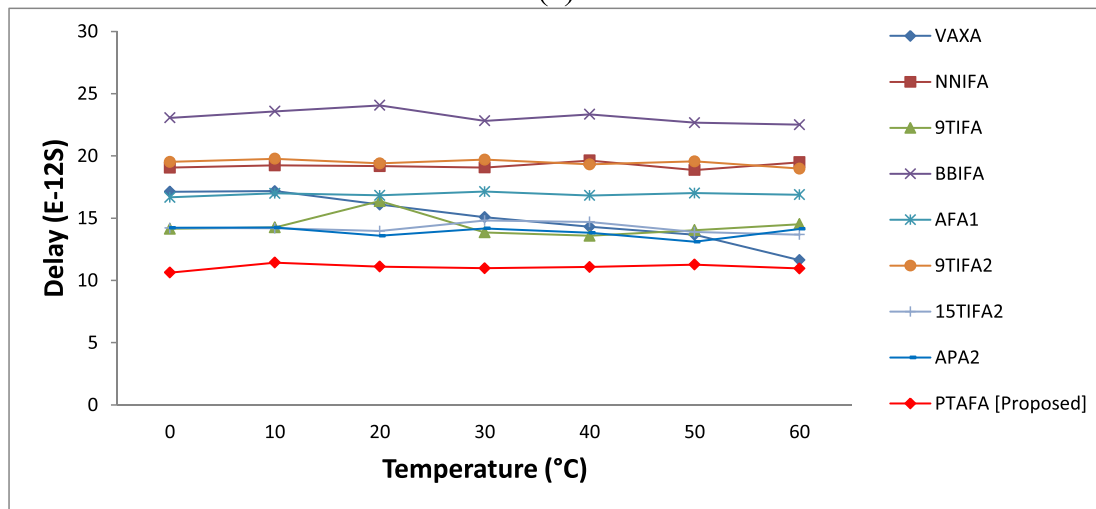
5.2. Application level

From an accuracy point of view, the efficiency of the approximate full adder cells is investigated in an image processing application. Image blending is chosen to apply an 8-bit adder which is composed of eight full adder cells. The lower half of the adder consists of inaccurate full adder cells, while the higher half consists of accurate cells. The block diagram of the image blending system is illustrated in Fig. 14. In Fig. 14, I_1 , I_2 , and α denote the first image, the second image, and the blending ratio. The blending ratio which is between zero and one determines the impact of I_1 on the final blended image. If $\alpha = 0$ then I_1 does not have any impact on the blended image. On the other hand, if $\alpha = 1$ then only I_1 forms the blended image. Otherwise, both input images will construct the final image regarding the blending ratio.

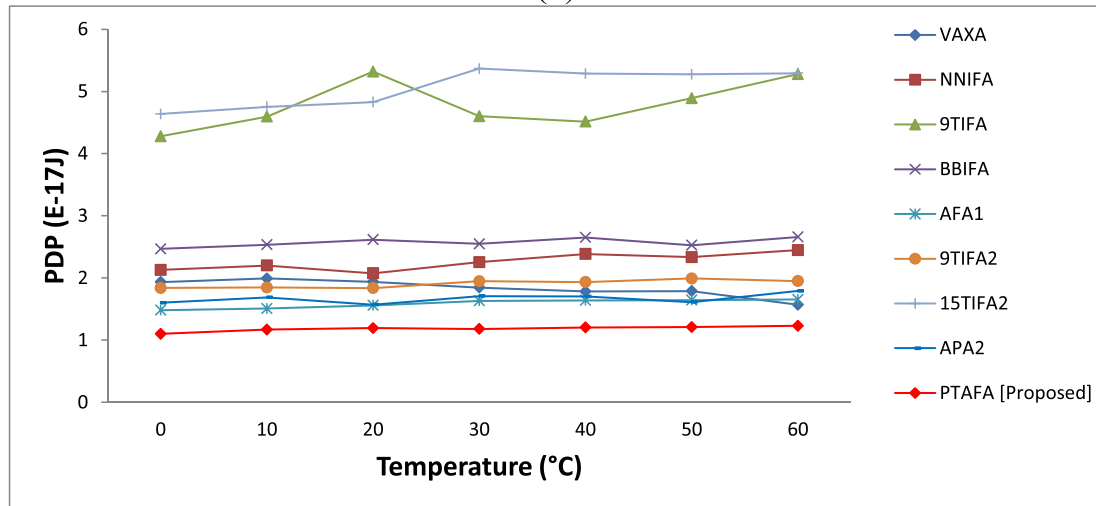
The image blending system is implemented using the MATLAB tool. In grayscale images, each pixel consists of an 8-bit unsigned binary digit. Therefore, an 8-bit word length adder is needed to add corresponding pixels in I_1 and I_2 images. We have written functions for each full adder cell based on their truth table. For the lower half of the adder, we call functions of approximate full adders but for the higher half, functions of accurate full adder cells are called. Simulation results of image blending application for three blending ratios including 0.1, 0.5, and 0.9 are demonstrated in Fig. 15. According to the results of this simulation, there is not a significant difference between the images obtained from the approximate 8-bit adder circuits and one can correctly infer output results.



(a)

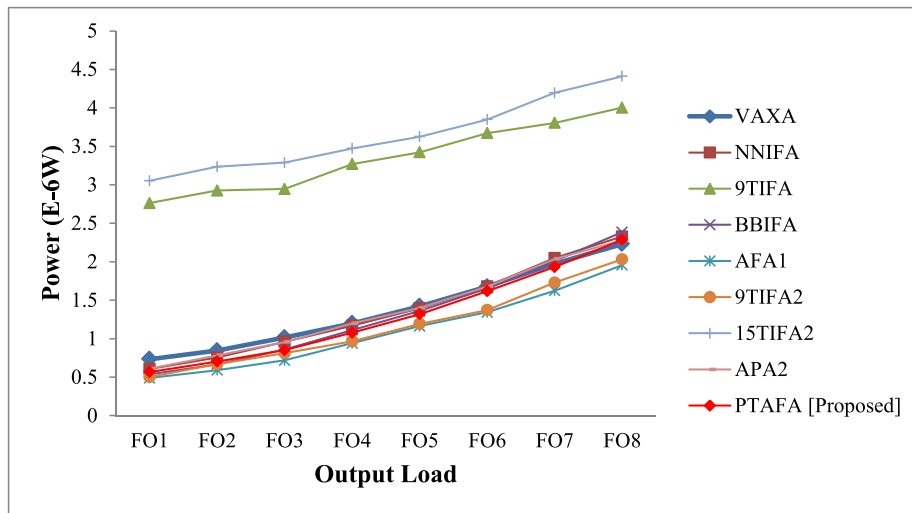


(b)

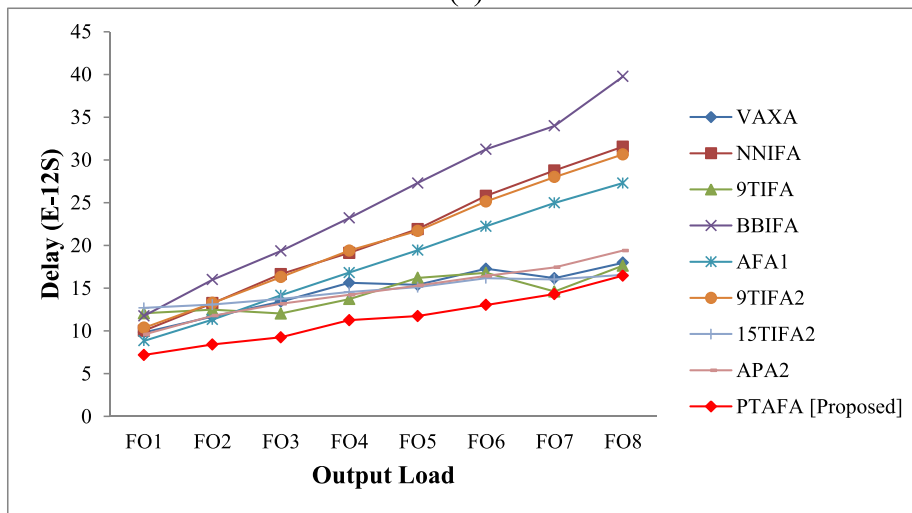


(c)

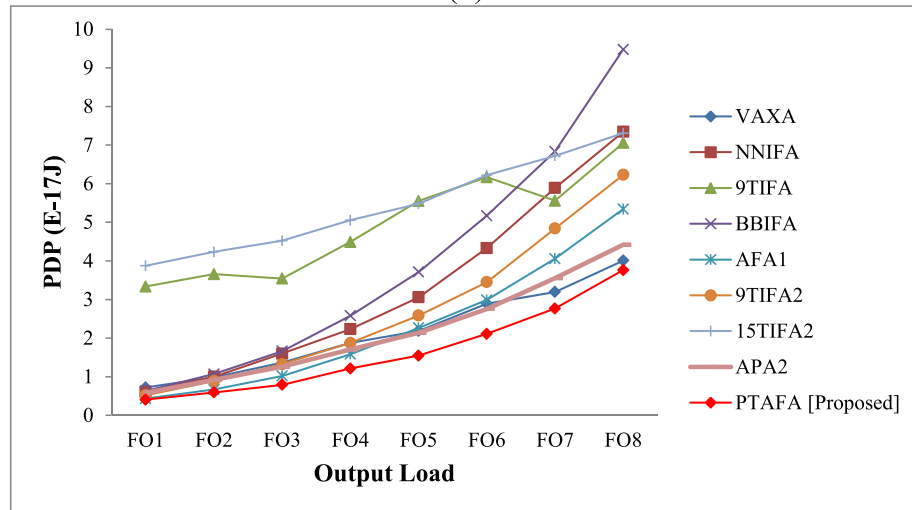
Fig. 12. Temperature scaling effects on (a) Power (b) Delay (c) PDP.



(a)



(b)



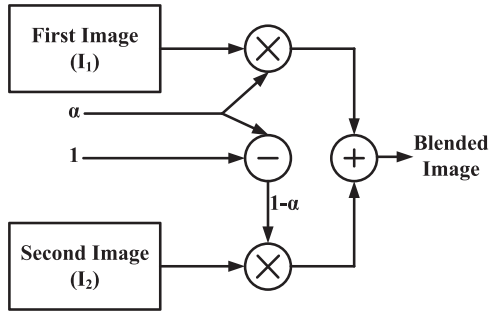
(c)

Fig. 13. Output load scaling effects on (a) Power (b) Delay (c) PDP.

Table 7

Mean, variance, and standard deviation values of the proposed cell against diameter deviations.

Diameter Deviations (nm)	0.05	0.10	0.15	0.20
Mean (μ)				
Power (E-6 W)	0.8423	0.8424	0.8421	0.8423
Delay (E-12 S)	16.90	17.13	17.50	17.83
PDP (E-16 J)	0.1423	0.1443	0.1474	0.1502
Variance (σ^2)				
Power (E-16 W)	0.0421	0.0882	0.1589	0.2198
Delay (E-25 S)	0.4093	1.797	3.442	5.813
PDP (E-35 J)	0.0030	0.0142	0.0260	0.0432
Standard deviation (σ)				
Power (E-8 W)	0.2052	0.2970	0.3986	0.4688
Delay (E-12 S)	0.2023	0.4239	0.5867	0.7624
PDP (E-18 J)	0.1749	0.3777	0.5100	0.6573

**Fig. 14.** Image blending application block diagram.

The peak signal-to-noise ratio (PSNR) is a well-known statistical metric defined in Eq. (16). It calculates the ratio of digital signal strength to destructive noise power which negatively affects the quality of the picture.

$$PSNR = 10 \log_{10} \left(\frac{MAX_I^2}{MSE} \right) \quad (16)$$

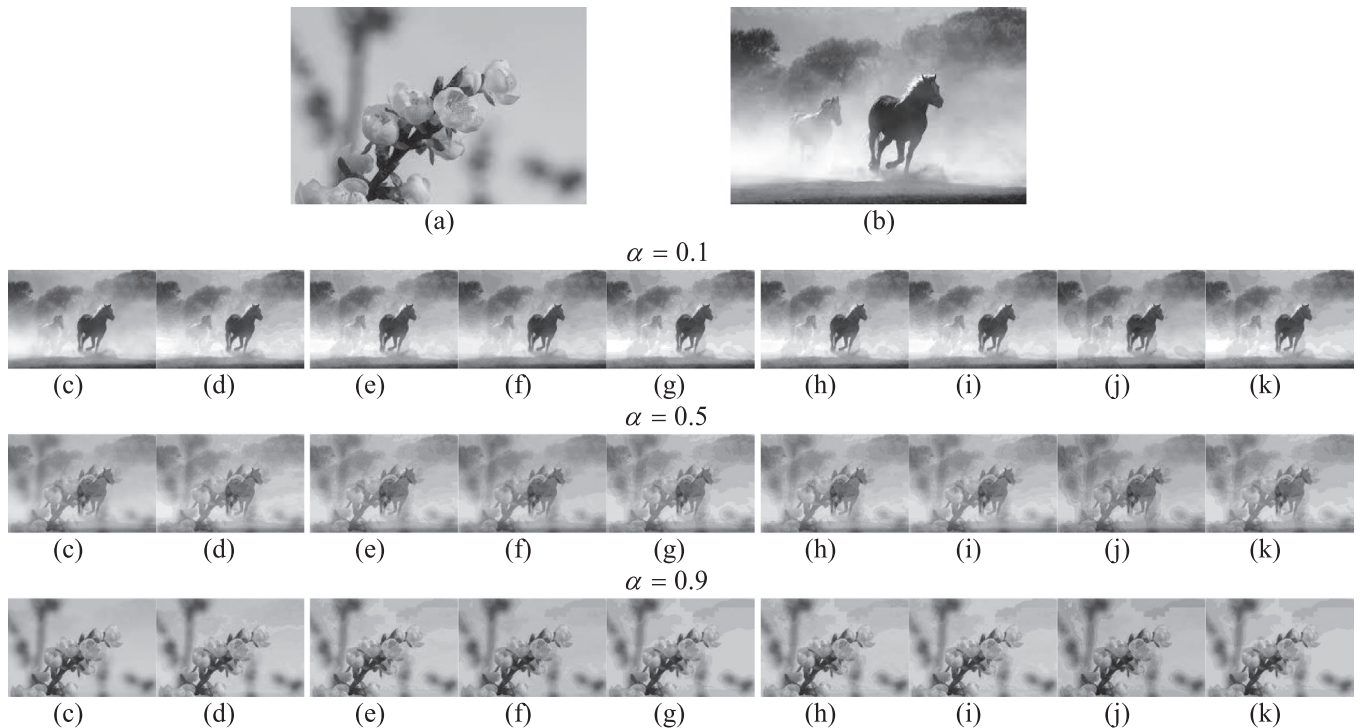
Where MAX_I and MSE denote the maximum value of the signal and mean squared error, respectively. Since each pixel's length is 8-bit, its maximum value is 255. The MSE metric is computed using Eq. (17).

$$MSE = \frac{1}{mn} \sum_{i=0}^{m-1} \sum_{j=0}^{n-1} [E(i,j) - I(i,j)]^2 \quad (17)$$

Where m and n denote the number of rows and columns of each output image. Also, E and I denote corresponding pixels of exact and inexact output images, respectively. A higher PSNR value indicates that the quality of the output image is better. Images with a PSNR above 30 dB are of good quality and acceptable [49]. Quantitative results of the image blending application for blending ratios of 0.1, 0.5, and 0.9 are shown in Fig. 16. As indicated in Fig. 16 (a), the PSNR value of the proposed PTAFA cell is higher than 30 dB regarding all values of blending ratio. The maximum and minimum values of the PSNR criterion belong to the VAXA and APA2 designs, respectively. Another well-known image quality metric is the structural similarity (SSIM) index which is used to predict the quality of reference and noisy image. It is based on human visual perception and considers similarities between two corresponding windows of images. Eq. (18) defines the SSIM metric. Further detailed information about the SSIM metric is presented in [50].

$$SSIM \left(x, y \right) = \frac{(2\mu_x \mu_y + C_1)(2\sigma_{xy} + C_2)}{(\mu_x^2 + \mu_y^2 + C_1)(\sigma_x^2 + \sigma_y^2 + C_2)} \quad (18)$$

The value of the SSIM is in the range of [0,1]. When the reference and sample images are the same then the SSIM is 1. When the SSIM value is 0 it indicates that the two images are very different. Hence, the higher value of the SSIM confirms the higher image quality. The SSIM quantitative metric of image blending simulation is depicted in Fig. 16 (b). The

**Fig. 15.** Image blending application (a) image I_1 (b) image I_2 (c) exact (d) VAXA (e) NNIFA, BBIFA (f) 9TIFA (g) AFA1 (h) 9TIFA2 (i) 15TIFA2 (j) APA2 (k) proposed PTAFA.

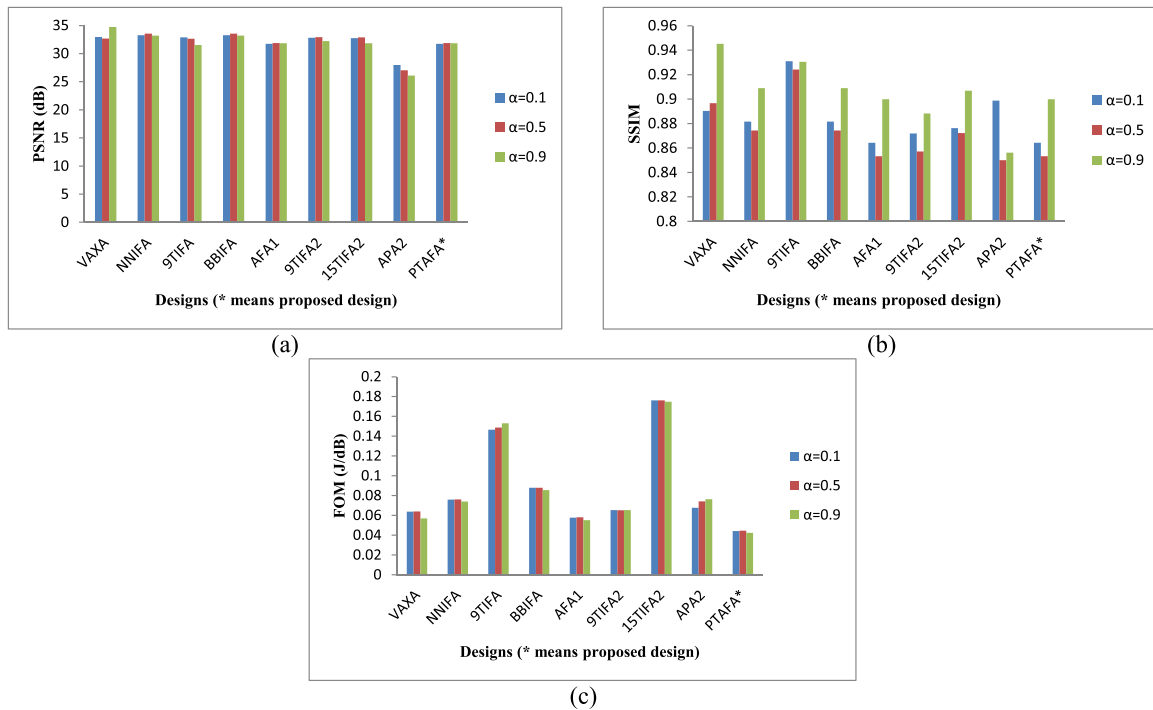


Fig. 16. Image processing quality metrics (a) PSNR (dB) (b) SSIM (c) FOM (J/dB).

highest SSIM belongs to the VAXA design. On the other hand, the lowest values of SSIM belong to the APA2 and 9TIFA2 designs, respectively. The proposed design has reasonable SSIM values for all image blending ratios.

Finally, to make a trade-off between hardware and application levels of abstraction we compare the efficiency of all designs using Eq. (19). It simultaneously considers energy consumption, PSNR, and SSIM metrics. This figure of merit provides a better insight into comparing different circuits. Some full adders decrease energy consumption while increasing output error. Therefore to have a fair comparison it is vital to consider both hardware and application level criteria. Since the energy consumption and error metrics are at the numerator and denominator parts of the fraction, respectively, the lower values of FOM indicate better results. Simulation results which are shown in Fig. 16 (c), confirm that the proposed PTIFA cell outperforms all designs and provides the lowest values.

$$FOM = \frac{Power \times Delay}{PSNR \times SSIM} \quad (19)$$

6. Conclusion

Multimedia processing algorithms are inherently error-resilient. There are portable applications that use video, image, or voice processing at the edge. Therefore, low energy and high-speed circuits are needed to increase battery lifetime and computation performance, respectively. Recently, the approximate computing paradigm has emerged as a solution to process data at the edge. The full adder cell is the heart of large arithmetic circuits. In this paper, we proposed a novel approximate full adder cell at the transistor level. The combination of pass transistor and transmission gate logic styles was used to design the proposed cell. To investigate the proposed design, extensive simulations at transistor and application levels were conducted. At the transistor level, the proposed design along with benchmarked circuits was assessed in terms of power consumption, latency, PDP, and EDP using the HSPICE simulator. All circuits under test were studied at various power supplies, ambient temperatures, and output loads at 32 nm CNFET technology node. Simulation results confirm the superiority of the proposed cell in

terms of latency, PDP, and EDP criteria. Also, the process variation of carbon nanotubes was investigated using Monte Carlo (MC) transient analysis. Considering MC simulation results, the proposed cell works correctly against diameter fluctuations of CNTs. At the application level, image blending was chosen to apply all approximate full adder designs to carry out an 8-bit addition operation and compare the quality of output images. Quantitative metrics such as peak signal-to-noise ratio (PSNR) and structural similarity (SSIM) index were taken into account. Considering these accuracy metrics, the proposed design works properly. Moreover, the switching and application-level metrics showed the effectiveness of the proposed cell in terms of FOM than the state-of-the-art.

CRedit authorship contribution statement

Akram Mohammadi: Conceptualization, Investigation, Validation, Visualization, Writing- Original draft preparation, **Mokhtar Mohammadi Ghanatghehstani:** Methodology, Software, Supervision, Investigation, **Amir Sabbagh Molahosseini:** Visualization, Project administration, Writing – Review & Editing, **Yavar Safaei Mehrabani:** Validation, Supervision, Project administration, Software, Writing – Review & Editing.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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